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Latency Measurements of Audio Sigma Delta Analogue to Digital and Digital to Analogue Converts

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ABSTRACT

Latency is a well recognised issue when using digital audio workstations for live music processing. Previous research has reported measurements of the latency of the whole audio processing chain based on a "blackbox" approach. This report presents the results of latency measurement of typical compact analogue to digital and digital to analogue converters (ADC/DACs) in isolation from computer system processing overheads by using a high-speed data acquisition device. The report discusses the testing methods and pitfalls. It confirms that the latency is almost exclusively accounted for by the expected group delay of the digital decimation filters and interpolation filters used in the Sigma-Delta convertor.

1 INTRODUCTION

Audio processing latency is a well known problem in live monitoring [1], real-time synthesis [2], and multi-channel live mixing etc. It is known from perceptual tests that the tolerable time delay for in-ear monitoring can be very low (less than 3-5ms) [1]. In computer based Digital Audio Workstation (DAW) systems the major latency (typically around 5 to 10ms) is caused by the buffer size [3], so the ADC/DAC converter latency is sometimes neglected or a rule of thumb of 1ms to 2ms is assumed.

Latency of professional digital consoles is normally under 2ms. Recording engineers are still concerned with latency caused by routing audio channel from digital console through various external analogue devices. In this case, the latency is mainly caused by additional ADC/DACs.

Previous reports have measured overall system latency based on a blackbox approach, especially on computer based DAW systems where the latency is more severe. However, this approach does not provide great help for latency management and compensation. It would be better to have accurate latency measurement of each stage of the whole audio processing chain.

Modern audios converters are commonly available in compact form by using one chipset to integrate both multichannel ADC and DAC, which is known as a hardware Codec. That can be found in computer motherboards and USB soundcards. They normally operate at relatively high frequency in order to multiplex multiple audio channels.
The most commonly used compact architecture for audio range converter is based on multi-bit sigma-delta modulators (SDMs). Accurate latency values for these convertors are not normally available and cannot be easily measured, although it is well known that this latency is mainly due to the group delay of the SDM's internal digital decimation and interpolation filter. The

group delay of the digital filter is expressed in a variety of formats in manufacturer's datasheets, quite often as a function of the number of samples divided by the sampling frequency.

2 THE LATENCY TEST FOR HARDWARE AUDIO CODECS

2.1 Testing platforms and devices

The tested audio converters are listed in Table **1**. They are all single chipset that integrate multiple ADC and DAC channels with available group delay data from datasheet. The protocols supported by these devices are typically used in most embedded audio systems and computer based system.

Table 1 List of Testing Systems

Code	Model	System	Protocol
(a)	TLV320-AIC23B	TMS320VC5510 DSK	McBSP
(b)	AD1836A	ADSP-21161N EZ-KIT Lite	TDM/I^2S
(c)	AD1981B	PC	AC'97
(d)	AD1882	PC	HD Audio

The Multichannel Buffered Serial Ports (McBSP) supported by codec (a) is software configurable protocol that supports various I^2S frame formats. Overall, all tested devices use standard serial transfer digital audio interfaces with multichannel support by Time Division Multiplexing (TDM) technique.

The purpose of the test is to evaluate the latency caused by the ADC and DAC of computer based DAWs. The most popular on-board audio subsystem are based on Audio Codec '97 (AC'97) standard or the Intel HD Audio standard, which are evaluated by devices (c) and (d). Devices (a) and (b) have similar architectures and supporting protocols that can be found in external audio interface cards or other compact professional audio systems.

2.2 The Testing Method

The pervious latency tests rely on comparing the offset between input and output signals of the system. However this method cannot be used for codec latency testing. Normally, codecs provide an internal analogue loopback circuit to support a "listen to input" feature for low latency applications such as audio monitoring. To the best knowledge of the authors, codecs seldom implement digital loopback. Therefore, we cannot treat the codec as blackbox and obtain the latency value of ADC and DAC by directly measuring the time domain signal offset from analogue inputs and outputs. The measurement has to be carried out by comparing analogue stimuli and their digital binary patterns.

The test is performed by directly probling the two test points of the analogue input pin and digital data output pin for the ADC module, or the analogue output pin and digital data input pin for the DAC module, using a high speed data acquisition tool. The testing method is depicted in Figure **1**.

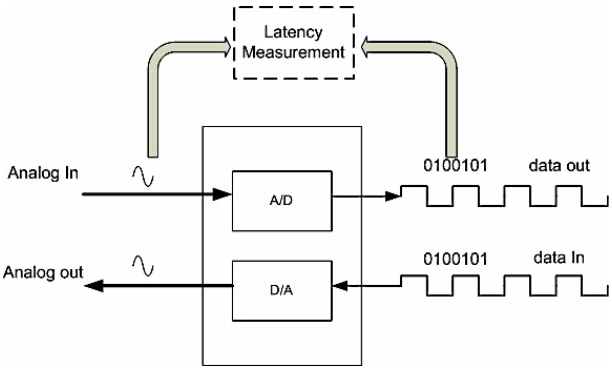

Figure 1 Codec latency measurement method

The multichannel features are supported by multiplexing samples in a digital serial data link. So the clock rate of the bit stream is normally much higher than the sampling frequency in order to support this feature. The range of codecs we tested have bit stream clock rate varying from 12MHz to 48MHz. Because we need to observe the change of binary pattern, a high time resolution is needed to interpret the binary data. Therefore, the National Instrument high speed data acquisition module NI PXI-5114 is used to support up to 250M samples pre second.

The digital data is represented internally with two's complement. It is relatively easy to test DAC latency, because the digital data can be clearly defined by software such as discrete impulse signal (a series 0s which has only one "1" inserted). Hence the clear binary pattern change can be captured, with observable "sinc function" like impulse output in the corresponding analogue pin.

It is more of a problem to measure ADC latency, the test signal needs to be considered so that the binary pattern change can be clearly identified. The noise interferences around the reference point zero can easily make binary pattern flips between all zeros and all ones. Therefore, we select the step input, which steps from the most

negative to most positive voltage according to the codecs' electrical characteristics.

2.3 The limitation of the test

The selection of the measuring point affects the accuracy of the measured values. The analogue measure point is selected as 90% of the final step value to indicate the "change" of the signal.

Most codecs input and output the digital stream in frame mode, and multiplex the multichannel samples inside a single frame. Therefore the selection of a binary pattern to reflect the analogue signal change might affect the accuracy around ± the frame time. For example if the frame rate is 48k Hz, then reading error might be 20.8 ± s.

Some protocols such as Intel HD audio uses fixed frame speed at 48K data bus to delivery different sampling frequencies. It will cause the uneven timing point of samples when measuring the digital end [4].

3 TESTING RESULTS AND DISCUSSIONS

The latency of a codec is mainly caused by the group delay of internal digital decimation and interpolation filters. However, sometimes manufactures don't provide details or completed information. Table **2** shows the available group delay information of tested codecs. They don't have the same format and sometimes they are hard to follow due to lack of details.

Table 2 Group delay of codec obtained from datasheet

Codec	Group Delay		Notes
	ADC	DAC	
(a)	(12, 20, 3, 6) / Fs	(11, 18, 5, 5) / Fs	Filter type (0, 1, 2, 3)
(b)	990.20 s	446.35 s	At sampling frequency 44.1kHz
(c)	16 / Fs	16 / Fs	
(d)	20 / Fs	20 / Fs	Typical value

The codec (a) provides the group delay information in number of samples according to different internal filter types. The filter type can be determined by codec register setting for different operation modes and sampling frequencies. In this case, codec (a) provides the most completed information among the codecs we tested.

The codec (b) provides the typical group delay in microseconds at sampling frequency of 44.1k Hz for both digital decimation filter in ADC and interpolation filter in DAC. However we don't know whether the filter varies when different sampling frequency is used.

The codec (c) provides overall delay as a function of sampling frequency with fixed 16 samples. From the measured results shown later, we assume that the 16 samples is for both decimation filter and interpolation filter. The codec (d) provides similar information as codec (c), with the typical delay of 20 samples. Apart from the same problem as codec (c), it also shows that the maximum delay can be -100 samples, which is hard to interpret.

Therefore the theoretical latency caused by group delay at typical sampling frequency 48k Hz, which can be summarised in Table **3** below:

Table 3 manufacture group delay data and equivalent latency at 48k Hz sampling frequency

Codec	Group Delay (samples)		Equivalent Delay (s)	
	ADC	DAC	ADC	DAC
(a)	12	11	250	229
(b)	44	20	917	417
(c)	16	16	333	333
(d)	20	20	417	417

Table **4** shows the measured latency values in microseconds. The measured latency values are correlated with reported group delay values. However the measured latency in some cases is longer than the group delay. The measured latency can be around 7 samples more than datasheet group delay.

We keep the decimal point of estimated samples due to the group delay caused by multi-stage decimation or interpolation filter. It can be normalised at the final sampling frequency with a fractional number of samples.

Table 4 Measured latency in microseconds at 48k Hz

Codec	Latency (s)		Equivalent Delay (samples)	
	ADC	ADC	DAC	DAC
(a)	308	275	14.8	13.2
(b)	1001	550	48	26.4
(c)	335	364	16.1	17.5
(d)	516	553	24.8	26.5

The decimation and interpolation filters can be different at different sampling frequencies. Table **5** shows the measured latency at different sampling frequency for the Intel HD codec (d).

Table 5 Latency in microseconds at different sampling frequency and equivalent samples for HD Audio Codec

Fs (kHz)	Measured Latency(s)		Equivalent Delay (samples)	
	ADC	DAC	ADC	DAC
32	748	853	23.9	27.3
44.1	562	620	24.8	27.3
48	516	553	24.8	26.5
96	283	288	27.2	27.7

It is worth to noting that the 44.1kHz data stream of the Intel HD audio protocol is delivered at 48kHz frame rate by only delivering 147 samples per 160 sample slots. Therefore the latency measurement of the digital data end has inherent deviations.

4 CONCLUSION

The test results show that the current hardware audio codec in both analogue to digital and digital to analogue direction will cause the latency range from around half millisecond to 1.5 milliseconds. The current datasheet information of group delay is either lacking of details or hard to use for estimation of sample accurate latency values. It is suggested that the latency information of an ADC/DAC needs to be available in standard and accurate format.

Some protocols designed for multiplexing channels make data bus delivery timing different from sampling frequency. This architecture might cause the problem for sample accurate live audio systems with minimum sample buffers.

Most decimation interpolation filters are implemented using multistage linear FIR structures. This delay could be reduced by adopting a different digital filter structure, such as a minimum phase filter with trade off of non-linearity [5].

It would be beneficial to have the facility to report the latency of a hardware audio codec to the up-layer software stack. For example, the simplest facility can be the digital loopback between ADC and DAC, which bypasses the up-layer audio driver and operating system. It would be interesting to see whether the advanced Built-In Self Test (BIST) architecture can be designed to automatically report latency of converters [6].

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6 REFERENCES

[1] M. Lester, J. Boley, “The Effects of Latency on Live Sound Monitoring”, Audio Engineering Society Convention Paper 7198 Presented at the 123rd Convention 2007 October 5–8 New York, NY, USA

[2] M. Wright, R.J. Cassidy, and M.F. Zbyszynski. “Audio and gesture latency measurements on linux and osx”, In Proceedings of the ICMC, pages 423–429, 2004.

[3] Y. Wang, R. Stables, and J. Reiss. “Audio latency measurement for desktop operating systems with onboard soundcards.” In Audio Engineering Society Convention 128, 5, 2010.

[4] Intel, “High Definition Audio Specification, Revision 1.0a”, June 17, 2010.

[5] R. Schreier, and G.C. Temes, “Understanding delta-sigma data converters”, IEEE Press New Jersey, 2005.

[6] M.F. Toner, and G.W. Roberts, “A BIST scheme for a SNR, gain tracking, and frequency response test of a sigma-delta ADC” Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on. 1995.